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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,257	07/23/2003	Anand Murthy	042390P9490C	1032

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,257	MURTHY ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7-23-03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-23-03 & 10-10-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the preliminary amendment filed July 23, 2003.

Response to Remarks

The preliminary amendment filed July 23, 2003 has been entered and considered.

Priority

This application filed under former 37 CFR 1.60 lacks the necessary reference to the prior application. A statement reading "This is a Continuation of Application No. 10/002,465, filed 11-01-01, Patent No. 6,621,131." should be entered following the title of the invention or as the first sentence of the specification. Also, the current status of all nonprovisional parent applications referenced should be included.

Drawings

The drawings are objected to because the thin strip element between the spacers and the gate electrode, and the layer formed on the gate dielectric are not labeled in Figures 2-6. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 38-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not understood what includes an n- or p-dopant. Is it the layer or the channel between the source and drain recesses?

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 28-37 and as best understood of claims 38-39 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 of U.S. Patent No. 6,621,131. Although the conflicting claims are not

identical, they are not patentably distinct from each other because claims of the present application are broader the Patent No. 6,621,131, in regard to claim 28 of the present invention, Patent No. 6,621,131 discloses a semiconductor transistor, comprising: a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing; a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which: (a) includes a p-dopant; and (b) is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is larger than the first spacing so that a compressive stress is created between the source and the drain in the channel; a gate dielectric layer on the channel; and a conductive gate electrode on the gate dielectric layer.

In regard to claims 29-30, Patent No. 6,621,131 discloses the second material includes the semiconductor material and an additive, the difference between the first spacing and the second spacing being due to the additive, wherein the additive is germanium.

In regard to claims 31-32, Patent No. 6,621,131 discloses tip regions formed between the source and the drain with the channel between the tip regions, the tip regions being formed by implanting of dopants and excluding the additive, wherein the dopants of the tip regions are p-dopants.

In regard to claim 33, Patent No. 6,621,131 discloses a semiconductor transistor comprising: a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing; a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which: (a) includes an n-dopant; and (b) is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is smaller than the first spacing, so that a tensile stress is created between the source and the drain in the channel; a gate dielectric layer on the channel; and a conductive gate electrode on the gate dielectric layer.

In regard to claims 34-35, Patent No. 6,621,131 discloses the second material includes the semiconductor material and an additive, the difference between the first spacing and the second spacing being due to the additive, wherein the additive is carbon.

In regard to claims 36-37, Patent No. 6,621,131 discloses tip regions formed between the source and the drain with the channel between the tip regions, the tip regions being formed by implanting of dopants and excluding the additive, wherein the dopants of the tip regions are n-dopants.

As best understood in regard to claim 38, Patent No. 6,621,131 discloses a semiconductor transistor comprising: a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a

semiconductor material having a first lattice with a first structure and a first spacing and at least the channel, including an n-dopant; a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is larger than the first spacing, so that a compressive stress is created between the source and the drain in the channel; a gate dielectric layer on the channel; and a conductive gate electrode on the gate dielectric layer.

As best understood in regard to claim 39, Patent No. 6,621,131 discloses a semiconductor transistor comprising: a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing and at least the channel, including a p-dopant; a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is smaller than the first spacing, so that a tensile stress is created between the source and the drain in the channel; a gate dielectric layer on the channel; and a conductive gate electrode on the gate dielectric layer.

Although the conflicting claims are not identical, they are not patentably distinct

from each other because the claims are arguably broader than claim 1 of Patent No. 6,621,131 which encompasses the same metes, bounds, and limitations. Therefore, it would be obvious to eliminate the limitations of the narrower claims, since it has been held that omission of an element and its function and a combination where the remaining elements perform the same functions as before involves only routine skill in the art. See *In re Karlson*, 136 USPQ 184.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor transistors with source and drain recesses:

Candelaria (5,683,934)	Cha (5,970,329)
Chan et al.. (US 6,380,088 B1)	Gardner et al. (6,110,786)
Hsieh et al. (5,956,590)	Okoumé (4,952,993)
Rovedo et al. (US 6,391,703 B1)	Tanabe et al. (4,633,099)
Wu (5,994,747)	Xiang et al. (US 6,437,404 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
March 5, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800